MOTOROLA
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Application Note
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HORIZONTAL APC/AFC LOOPS

Prepared by
Linear Applications

The most popular method used in modern television receivers to synchronize the line frequency oscillator is the phase locked loop. Although in detail the circuits may vary considerably, the fundamental operation is the same. Any designer with a good understanding of phase locked loops in general and the required operating characteristics of television line frequency oscillators in particular, should be able to handle these circuits successfully.

For color television signal transmissions in the United States, the line frequency (f_H) is directly related to the color subcarrier frequency (f_{sc}) such that:

$$f_H = \frac{2Xf_{sc}}{455}$$

Since $f_{sc} = 3.579545$ MHz ± 10 Hz, then the line period is given by:

$$H = 63.5555 \pm 0.0002\ \mu s$$

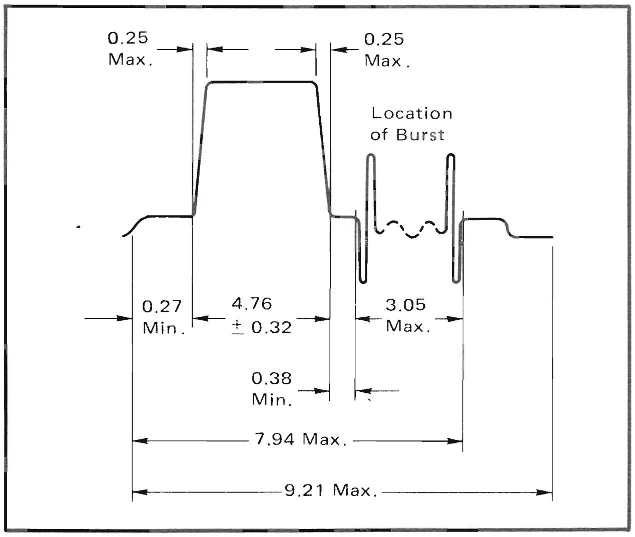

FIGURE 1 — Timing Detail of Line Sync Pulse (μs)

For satisfactory operating characteristics, the receiver must meet the following requirements:

1. **Dynamic Phase Accuracy:**

or—repetitive phase accuracy. If the phase of a scan line is shifted with respect to the preceding line, a loss of detail can occur. For a given video frequency, a half cycle error from line to line will cause a complete loss of information at that frequency. At the system limit of 4.5 MHz, this corresponds to a 0.111 μs timing error between adjacent lines or a repetitive phase accuracy of 0.62 degrees. Should thermal noise be present in the signal, the miss-timing will be masked and much larger phase errors are tolerable. (See later discussions on noise performance.)

2. **Static Phasing:**

or—static phase error with the line oscillator at nominal frequency (f_H). For monochrome receivers, this is determined by the tolerable shift of the picture information with respect to the raster and may be as much as 1.5 μs. For color receivers, it is generally much less ($< 0.5\ \mu s$) to permit gating the burst information on the back porch of the signal.

3. **Static Phase Error (with detuning):**

When the line oscillator is detuned from the nominal line frequency, the timing between the picture information and the receiver raster will change. For an inexpensive monochrome receiver, this error can be large (2 μs for $\Delta_f = 300$ Hz), particularly if the screen is overscanned and the picture escutcheon masks the sides of the raster. For a color receiver, the S.P.E. is usually smaller. Figure 1 gives the tolerance of the burst envelope on the signal back-porch and shows that the burst can occupy a 3 μs 'window' with respect to the leading edge of the sync pulse. The gating pulse for the burst channel is as narrow as possible to keep the chroma system noise bandwidth low and to prevent gating adjacent picture information or sync widgets. A gate pulse of 4 μs accurately centered when the line oscillator is at f_H will permit an S.P.E. of ±0.5 μs and yet maintain proper gating. Thus, for optimum performance, the S.P.E. over the detuning range of the line oscillator should be no more than ±0.5 μs.

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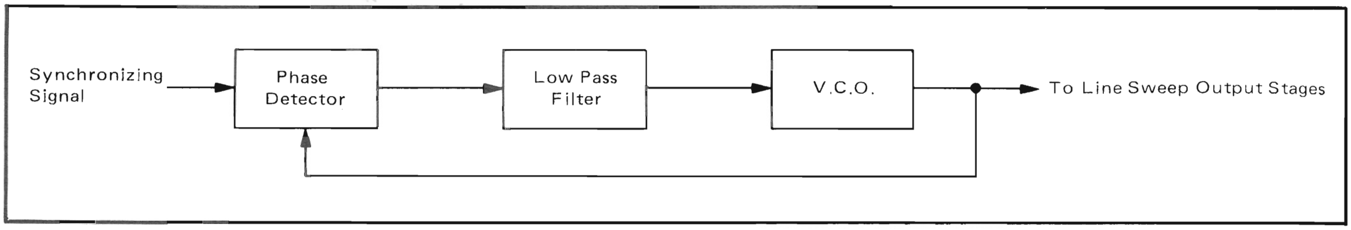

FIGURE 2 – APC/AFC Loop Theory

4. **Hold-In Range:**

This is the total frequency deviation from f_H over which an already synchronized oscillator will remain in synchronism, with no interruption of the synchronizing signal. This can typically be from 600 Hz to 800 Hz but is not usually designed for and occurs as the result of other design considerations.

5. **Pull-In Range:**

This is the total frequency deviation of the line oscillator from f_H over which the receiver will remain in synchronism, even following a momentary interruption of the synchronizing signal. Expressed another way, it is the limits of free-running oscillator frequency from which the oscillator will pull into synchronism on application of a synchronizing signal. The required pull-in range will depend on the frequency stability of the line oscillator and the permissible static phase error. It is usually $>\pm 180$ Hz.

6. **Pull-In Time:**

The time taken to synchronize from the limits of the pull-in range. Anything less than 1 second is considered instantaneous.

Four parameters are of primary interest; the phase detector sensitivity, the oscillator sensitivity, the loop gain, and the filter transfer characteristic.

1. **Phase Detector Sensitivity (μ):**

The phase detector compares the incoming synchronizing signal with the line frequency oscillator signal and develops a control voltage that is proportional to the magnitude and polarity of the phase difference between the signals. If for a given phase difference at the phase detector of $\delta\phi$ a control voltage δE is generated, then the phase detector sensitivity is defined as:

$$\mu = \frac{\delta E}{\delta\phi} \text{ and is usually measured in volts/radian.}$$

Since we are dealing with rectangular sync pulses and the signal from the oscillator is usually integrated to form a linear ramp, the phase detector output

$$E = \mu\phi$$

This is true over the stable operating region of the phase detector. (For further discussion of the stable and unstable operating regions, see Pull-In Range calculation on page 6.)

2. **Oscillator Sensitivity (β):**

If a voltage δE at the control terminal of the oscillator produces a change of δ_f in the free-running frequency of the oscillator, then the oscillator sensitivity (β) is defined as:

$$\beta = \frac{\delta_f}{\delta E} \text{ and the usual units are hertz/volt.}$$

3. **D.C. Loop Gain (f_c):**

When the oscillator has a tuning error of Δ_f Hz, then the required correction voltage at the control terminal of the oscillator is Δ_f/β. If the system is capable of producing this correction voltage, the oscillator will remain in synchronism and the output voltage from the filter will be d.c. If the filter has a d.c. transmission of 100%, the phase detector output is Δ_f/β and a static phase error of ϕ will exist between the inputs of the phase detector to maintain this voltage.

$$\therefore \mu\phi = \Delta_f/\beta$$

$$\text{or } \phi = \frac{\Delta_f}{\mu\beta} \qquad ①$$

The quantity $\mu\beta$ is defined as the d.c. loop gain (f_c) although its units are Hz/rad.

It is clear that the S.P.E. is directly proportional to the error in oscillator free-running frequency and is inversely proportional to the d.c. loop gain. The S.P.E. can be made as small as desired for a given tuning error by increasing the d.c. loop gain. However, note that the phase error ϕ thus far defined is the static or long term phase error. To determine the dynamic phase error, i.e., the effect of impulse or thermal noise of the loop performance, we must evaluate the loop filter characteristics.

4. **Filter Transfer Characteristic $F_{(p)}$:**

The low pass filter connected between the phase detector and the oscillator will have a significant effect on the loop performance. As this part of the system is the one most open to design adjustment, it should be fully understood. If single time-constant networks are used, it

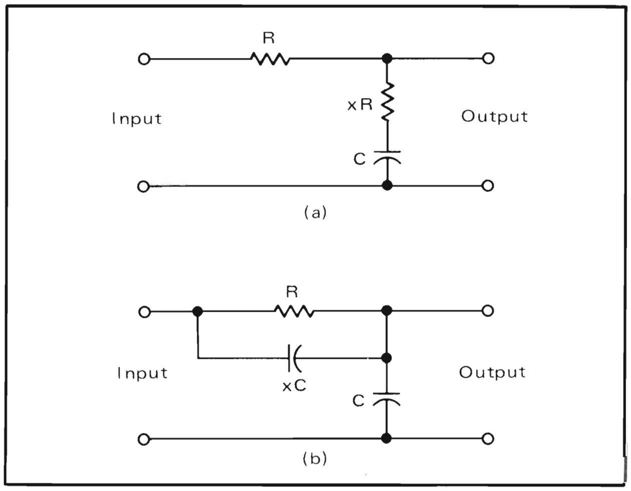

FIGURE 3 – Typical Filter Networks

becomes impractical to achieve both small S.P.E.'s and small dynamic phase errors (low noise bandwidths) since the former requires a large value for f_c and the latter a small value for f_c. To avoid this compromise, more elaborate networks are used.

Both a) and b) are equivalent "proportional plus integral" networks. The output control voltage is proportional to the current through R plus the integral of the current in C. At any frequency, the ratio of the output voltage to the input voltage is:

$$F_{(p)} = \frac{1+pT_1}{1+pT_2} \quad \text{where} \quad \begin{array}{l} T_1 = xRC \\ T_2 = (1+x)RC \end{array}$$

$$\therefore F_{(p)} = \frac{1+pxRC}{1+(1+x)pRC} \qquad \textcircled{2}$$

At d.c., the filter transmission $F_{(p)} = 1$ and at high frequencies, the above expression reduces to $\frac{x}{x+1}$

$$\therefore \frac{AC}{DC} \text{ gain ratio } m = \frac{x}{x+1}$$

The parameter m becomes important in the design of satisfactory loops.

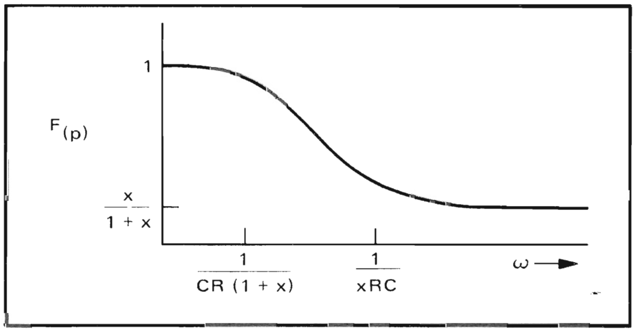

FIGURE 4 — Filter Frequency Characteristics

5. Dynamic Phase Error or Noise Bandwidth:

Noise can be specified by its energy content and for a flat energy spectrum impulse noise and thermal noise are quite distinct. The relative phases of the frequency components of impulse noise are related and not random, although occurrence is a random variable. For thermal noise, the relative phases of the frequency components are completely random and incoherent and this type of noise is the most difficult to reject. Therefore, most of the following treatment is concerned with the rejection of thermal noise. However, methods to minimize the effects of impulse noise are also covered below in the selection of the filter components.

The presence of thermal noise in the signal will cause random variations in the output phase of the voltage controlled oscillator. An excellent way of determining the ability of the APC loop to reject thermal noise is to measure the noise bandwidth. This can be done by assuming a noise free input phase which has sinusoidal variation with time and calculating the corresponding output phase. If this is repeated over a range of frequencies, the bandwidth for which the loop has significant variations in output phase can be determined, i.e., the noise bandwidth has been found.

For a loop that is initially phase locked, if the input phase changes to ϕ_i with a corresponding output phase change of ϕ_o, the resulting phase error of the system

$$\phi = \phi_i - \phi_o$$

and the phase detector output voltage is $\mu\phi$.

For a filter transfer function of $F_{(p)}$, the oscillator control voltage becomes

$$F_{(p)}\,\mu\phi$$

and the oscillator (with sensitivity β) will attempt to change frequency by

$$F_{(p)}\,2\pi\mu\beta\phi$$

If frequency lock is to be maintained, the frequency shift of the oscillator must match the rate of change of the filter output phase

$$\therefore p\phi_o = F_{(p)}\,2\pi\,\mu\beta\phi \qquad p = \frac{d}{df}$$

$$2\pi\,\mu\beta = 2\pi\,f_c = \omega_c$$

or

$$\boxed{p\phi + F_{(p)}\omega_c\phi = p\phi_i} \qquad \textcircled{3}$$

This is the general D.E. for APC/AFC loops although its use for the asynchronous condition is subject to certain restrictions given later.

$$\therefore \phi_i = \phi_o \left\{ 1 + \frac{P}{\omega_c F_{(p)}} \right\}$$

$$\therefore \text{The phase transfer ratio } \frac{\phi_o}{\phi_i} = Q_{(p)} = \frac{F_{(p)}}{F_{(p)} + P/\omega_c} \qquad \textcircled{4}$$

Now for either of the filters shown in Figure 3,

$$F_{(p)} = \frac{1+pxRC}{1+p\,(1+x)RC} \qquad \begin{array}{r} \text{putting } RC = T \\ P = j\omega \end{array}$$

$$\therefore Q_{(\omega)} = \frac{1+j\omega xT}{1-\omega^2(1+x)\,T/\omega_c + j\omega\,(xT+1/\omega_c)}$$

It is important to note the presence of ω_c in the above expression. While the filter can modify the control voltage applied to the oscillator, the final output phase will depend on the loop gain f_c. The S.P.E. can be modified for a given detuning by changing f_c alone. The dynamic phase error can be modified by changing either f_c or $F_{(p)}$, or both.

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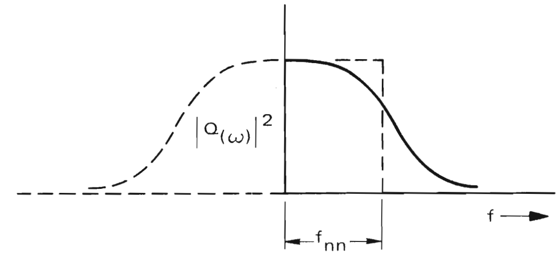


$$\text{Noise Bandwith } f_n = \int_{-\infty}^{+\infty} \left[Q_{(\omega)}\right]^2 df$$

The equivalent noise bandwidth is found by squaring the $Q_{(\omega)}$ curve and finding the rectangular bandwith of the same height enclosing the same area. (See also CER100, page 11.)

FIGURE 5

A plot of $Q_{(\omega)}$ against input frequency (noise frequency) will show the ability of the loop to reject thermal noise in the synchronizing signal.

The integration is carried out from $-\infty$ to $+\infty$ since the abscissa does not represent the absolute frequency of the noise but the difference frequency between the noise and the oscillator frequency as detected by the phase detector. The phase detector output does not distinguish between frequencies above or below the oscillator frequency. A term commonly used for APC loops is the noise semi-bandwidth f_{nn}.

$$f_{nn} = \frac{f_n}{2} = \int_0^\infty \left|Q_{(\omega)}\right|^2 df$$

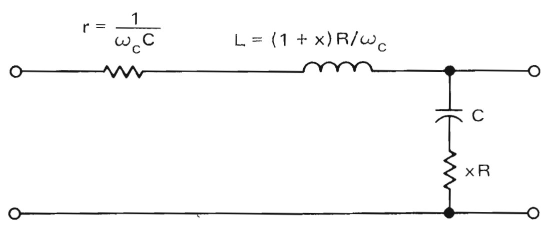
$$\left[Q_\omega\right]^2 = \frac{1 + \omega^2 x^2 T^2}{\left[1 - \frac{\omega^2}{\omega_c}(1+x)T\right]^2 + \omega^2\left[xT + 1/\omega_c\right]^2}$$

$$\therefore f_{nn} = \frac{\omega_c\left[1 + \frac{x^2 T\omega_c}{(1+x)}\right]}{4(1+xT\omega_c)} \qquad ⑤$$

6. Other Synchronized Loop Characteristics:

It should be clear from ⑤ above that if $x \neq 0$ (1) for a given value of d.c. loop gain to produce satisfactory static phase performance, two parameters are available to produce satisfactory dynamic phase performance (x and T).

To obtain an idea of the best way to vary these parameters, assume that ϕ_i and ϕ_o are the voltage input and output of a low pass filter (Figure 6).



$$\phi_o/\phi_i = Q_{(p)} = \frac{\frac{1}{PC + xR}}{1/C\omega_c + P(1+x)R/\omega_c + 1/PC + xR}$$

FIGURE 6 — Equivalent Voltage Transfer Filter

Step inputs to this filter can easily cause ringing. The output, following a step change in input phase (from signal source switching or a temporary spike of impulse noise) will assume a steady state following a transient.

$$\text{Now, } Q_{(p)} = \frac{\phi_o}{\phi_i}$$

The steady state (particular solution) is $\phi_i - \phi_o = \phi$. The transient (complementary function) is given by:

$$\frac{1}{Q_{(p)}} = 0$$

i.e., $\quad (1+x)Tp^2 + (1+xT\omega_c)p + \omega_c = 0$

Solving for p, we have:

$$P = \frac{-(1+xT\omega_c) \pm \sqrt{(1+xT\omega_c)^2 - 4(1+x)T\omega_c}}{2(1+x)T} \qquad ⑥$$

The real part of ⑥ will give the natural undamped resonant frequency of the loop.

$$\boxed{\omega_n = \frac{\sqrt{4(1+x)T\omega_c}}{2(1+x)T} = \sqrt{\frac{\omega_c}{(1+x)T}}} \qquad ⑦$$

The quantity under the root sign in equation ⑥ will determine the response of the loop to a step input. For critical damping, this quantity will be zero.

$$(1+xT\omega_c)^2 = 4(1+x)T\omega_c$$

If we define a damping coefficient $K = \frac{(1+xT\omega_c)^2}{4(1+x)T\omega_c}$ ⑧

then, K = 1 and the loop is critically damped.

K > 1 and the loop is overdamped.

K < 1 and the loop is underdamped and a period of oscillatory ringing will occur.

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(1) If the filters of Figure 3 are simplified by pulling x = 0, then eq. ⑤ reduces to $f_{nn} = \frac{\omega_c}{4}$. Since $\phi = \frac{\Delta\omega}{\omega_c}$, then $f_{nn} = \frac{\Delta\omega}{\phi}$.

Thus with x = 0 and a given detuning error, the S.P.E. and f_{nn} cannot be chosen independently.

The values of ω_n and K will have a significant effect on the loop synchronous performance. If ω_n is low $K > 1$, the system may take an appreciable time to reach a stable state following a change of input phase. Therefore, there will be little transient disturbance from impulse noise because of the sluggish reaction of the loop. However, if the input phase changes as a result of airplane flutter, the loop may respond too slowly to produce satisfactory tracking of the input signal. Also, the pull-in from an asynchronous condition may be sloppy and slow. Conversely, if ω_n is increased and $K < 1$, the loop can respond very rapidly to incoming phase changes, but may be unstable with oscillatory ringing when impulse noise is encountered. Suitable design values will depend on the required characteristics and the interaction of the APC loop with other subsystems in the receiver and these will be discussed in detail later. In general, it can be assumed that $x << 1$ and $xT\omega_c >> 1$ so that the formulae derived above can be simplified.

$$\left.\begin{array}{ll} \phi = \frac{\Delta f}{f_c} & \textcircled{1} \\[2ex] f_{nn} = \frac{1 + x^2 T\omega_c}{4xT} & \textcircled{5} \\[2ex] \omega_n = \frac{\omega_c}{(1+x)T} & \textcircled{7} \\[2ex] K = \frac{x^2 T\omega_c}{4} & \textcircled{8} \end{array}\right\} \textcircled{9}$$

7. **Asynchronous Performance of the Loop:**

As the tuning difference (Δf) between the oscillator free-running frequency and the incoming synchronizing signal increases, a larger static phase error is required at the inputs to the phase detector to maintain synchronism. Eventually, the phase detector output will stop increasing as the S.P.E. increases and the limit of hold-in will be reached(2). Should a further increase in Δf occur, the system becomes unstable and falls out of lock.

When the loop is out of synchronism, the phase detector will have two regions of operation (see Figure 7). If the sync pulse coincides with the steep slope of the integrated pulse from the V.C.O., this is the normal or stable operating region. The loop gain (f_c) is large and positive. When the sync pulse coincides with the more shallow slope of the sawtooth, operation is in the unstable region and the loop gain is much lower and negative.

Notice, however, that the phase detector outputs always operate to reduce the period of the beat note produced by the frequency difference between the sync and sawtooth. Hence, the beat note is very asymmetrical and has an average d.c. output at the filter terminal. As Δf decreases, the average d.c. voltage will build up on the filter capacitor until pull-in is achieved.

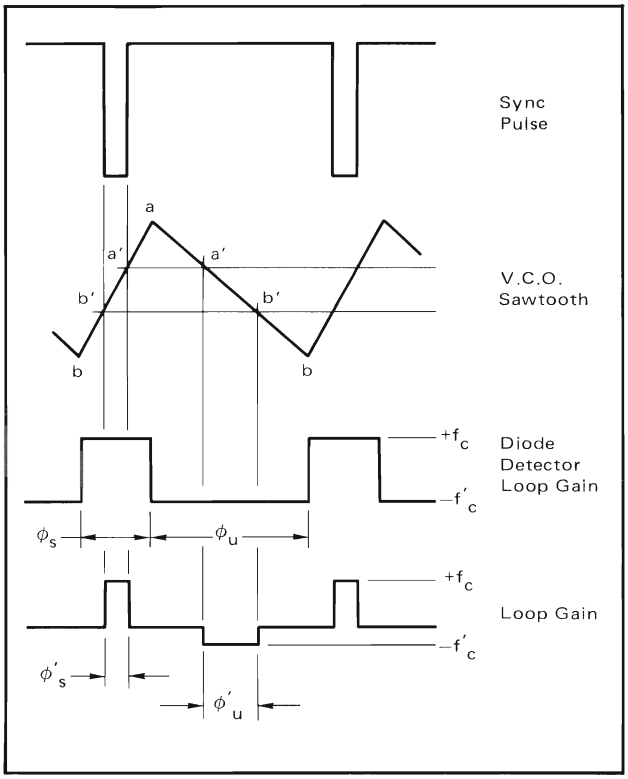

FIGURE 7

If the maximum output from the phase detector is ±E (obtained at points a and b on the sawtooth), then for the stable regions

$$f_c = \frac{2\,\beta E}{\phi_s}$$

and for the unstable region ϕ_μ

$$-f'_c = \frac{2\,\beta E}{\phi_\mu}$$

$$\therefore f_c\phi_s = f'_c\phi_\mu$$

Two assumptions are implicit in the above: (1) the oscillator sensitivity (β) remains constant over the range of control voltages produced by the phase detector, and (2) the integrated fly-back pulse is a linear ramp. For a typical diode bridge phase detector, the width of the narrow slope of the sawtooth is the stable region. However, the above expressions will still hold even if this is not the case. Should the phase detector output limit at a′ and b′ on the slope, the areas under the loop gain curve are reduced

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(2) The Static Phase Error $\phi = \frac{\Delta f}{f_c}$ and $\phi\text{max.} = \frac{\phi_s}{2}$

(ϕ_s = width of stable operating region of the loop.)

$$\therefore \text{Maximum hold-in range } \Delta f_{max.} = \frac{f_c\phi_s}{2} \quad \textcircled{10}$$

correspondingly with new stable and unstable regions ϕ'_s and ϕ'_μ (this limitation could also be caused by the inability of the oscillator control to change the oscillator frequency close to the peak phase detector output voltages). For an integrated circuit phase detector, the MC1391, the phase detector output is limited to the sync-pulse width since it is a sync-gated system, i.e., $\phi_s = 4.75\ \mu s$.

When the loop is out of lock, a steady beat note output results from the phase detector. For a simple resistive filter (with no capacitors), the beat frequency would be constant and no pull-in would occur, but for the filters of interest the d.c. component of the waveform tends to reduce the mean tuning error. Thus at any time, the free-running frequency of the oscillator in the absence of syncs will be greater than the off-set frequency obtained when the loop is closed. Notice, however, that as the detuning error increases, the waveform becomes more sinusoidal, reducing the d.c. component and the pull-in effect. Should the mean value of the d.c. component be found in terms of its frequency shifting capability, we can find the pull-in range and the pull-in time from any frequency within the pull-in range.

As shown in Appendix H, the maximum pull-in range Δf_{max} is given by:

$$\boxed{\Delta f_{max} = \frac{2\,\phi_s\,f_c\,\sqrt{m}}{(3+m)} \quad \text{———} ⑪}$$

if m << 1

The above expression, together with the formulae presented in ⑨, will completely specify the important characteristics of the conventional horizontal APC/AFC loop. The next section will cover the practical design use of these formulae, and detail instances of departure from the ideal case.

It should be apparent by now that the design of a satisfactory APC/AFC loop is not as straightforward as the simple block diagram of Figure 2 might have suggested. Five formulae are needed to define the characteristics of the loop and these formulae are not mutually independent. The designer has only three parameters that he can vary to fit all these formulae and meet his circuit needs. Further, his needs may change depending on the type and performance of circuits internal to the loop and, to complicate matters more, of circuits external to the loop. An obvious example of the former is the oscillator stability which will be a prime factor in determining the pull-in range required, and an example of the latter is the Static Phase Error permitted for correct burst gating in the chroma channel. If the burst is sync gated, then the S.P.E. requirement may not be as stringent although large oscillator drifts could result in high d.c. loop gain being needed that will also produce small S.P.E.'s.

Other factors that must be entered into the design concern the expected environment of the loop, both within the receiver and in the type and quality of the signals that will be received. Should the receiver manufacturer have a reputation for high performance in fringe reception areas, then he will be very concerned with thermal noise performance and the APC/AFC loop will tend to have small noise bandwidths. Alternatively, if the manufacturer is more concerned with urban reception, particularly near large airports, the loop will probably need to be high speed to track phase variations. More likely, the manufacturer will want the receiver to perform well everywhere and compromises must be made.

Within the receiver the characteristics of the loop will depend on the sync source and, for gated a.g.c. systems, the performance of the a.g.c. loop, especially when the horizontal oscillator is temporarily out of synchronism. Many loops use a dual diode arrangement for the phase detector and the sensitivity of this type of detector (see

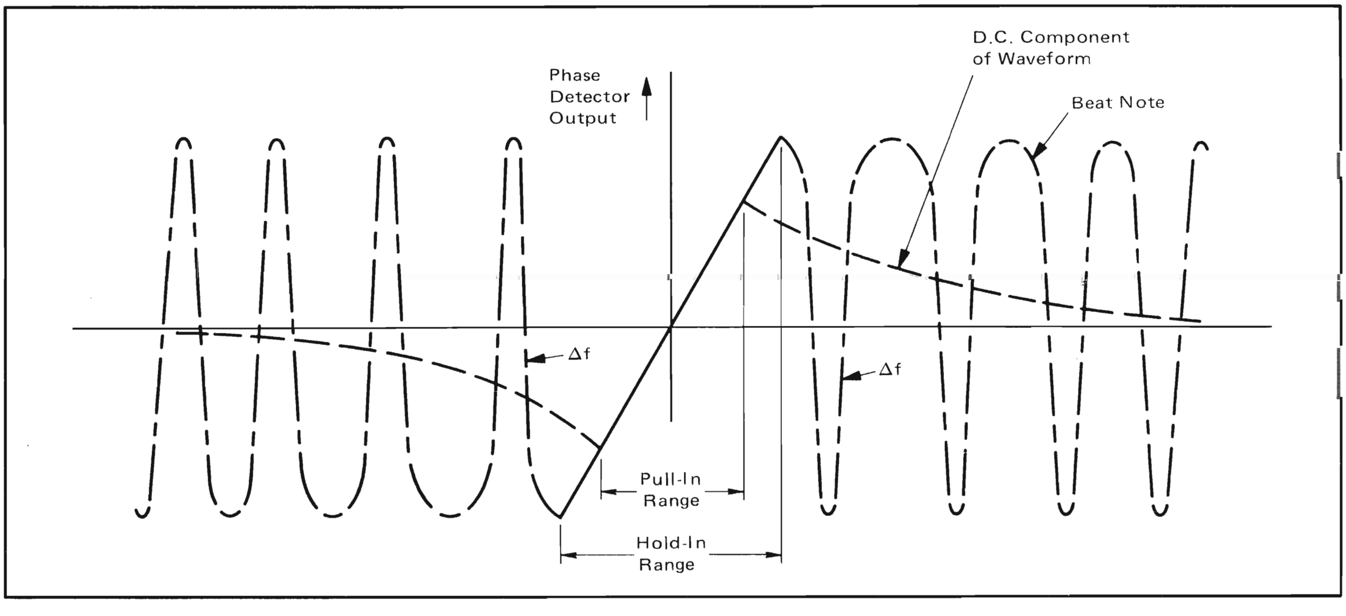

FIGURE 8 — Detector Beat Notes

Appendix) depends on the amplitude of the smaller of the two waveforms applied to it. The reference sawtooth waveform from the sweep circuit is usually chosen so that the phase detector sensitivity will not change with adverse signal conditions that affect the syncs. With a fixed oscillator sensitivity, the required d.c. loop gain can be obtained by changing the reference sawtooth waveform amplitude. For high loop gains and maximum flexibility, this means that the sync amplitude should be large—a requirement that can be difficult to meet in a 12 V. battery operated set. Alternatively, the effective amplitude of the sawtooth can be raised by using an active shaper network to increase the slope of the sawtooth.

A slow a.g.c. loop can seriously modify the apparent performance of the loop. If airplane flutter causes significant changes in the video detector output level and the sync separator is too slow to follow these changes, then the varying slice level will cause phase shifts at the input to the loop (see CER105). Also, when the line oscillator is out of lock, the gating pulse will activate the a.g.c. system during the video portion of the signal. This tends to make the a.g.c. loop increase the gain of the R.F. and I.F. amplifiers. Conversely, when the gate pulse and sync pulse coincide, the a.g.c. loop will attempt to reduce the R.F. and I.F. amplifier gains. The detector output that results from this process is modulated with a ripple corresponding to the frequency difference between the horizontal oscillator and the sync waveform. If the ripple amplitude is large then 'holes' will appear in the separated sync. The phase detector output beat note will be modified by these 'holes' and the mean d.c. voltage generated will be reduced causing a reduction in the oscillator pull-in range. This effect should be particularly noted when comparing a solid state receiver with an earlier tube or hybrid design. The introduction of I/C's into the receiver to perform the a.g.c. function (e.g., MC1345/44) has meant that coincidence of the sync and flyback pulse is necessary to gate the a.g.c. Since erroneous gating does not occur during the video portion of the signal, the detector level remains much more constant and wider pull-in ranges approximately the theoretical maximum (equation 11) are obtained.

A popular method of assessing the pull-in range is to offset the oscillator while syncs are applied to the loop. The 60 Hz component in the sync waveform is usually enough to cause a side-lock at multiples of the field frequency and the pull-in range is noted as the last side-lock on either side of 15.734 KHz from which the oscillator pulls into synchronism. Since the ripple at the detector increases as the oscillator approaches 15.734 KHz (the a.g.c. gate samples video for longer periods), the APC/AFC loop will get very little sync information and the beat note pull-in effect is correspondingly weak. Thus, for a tube design, the pull-in range obtained by the above method is close to the actual free-running frequency from which the oscillator can be locked. By measuring the picture offset on the CRT at the pull-in limits, the maximum stable phase error the system will tolerate is also found. However, with a solid state receiver using an improved a.g.c. system, a strong beat note (but no ripple at the detector) is generated when the APC/AFC loop is out of lock and the side-lock frequency limits at pull-in are significantly lower than the oscillator actual free-running frequencies at pull-in. Since the true pull-in range is not observed, the S.P.E. over the pull-in range obtained by the above method will be larger than a similar design with a poor a.g.c. system(3).

Another characteristic of the APC/AFC loop that will depend in a large measure on the external circuitry is the required noise bandwidth. The effect of random noise in the sync waveform is to cause the position of individual picture elements to vary from instant to instant. The larger dynamic phase error that can be tolerated will depend on many subjective factors. For example: At the same time noise appears in the sync waveform, it will also be present in the video masking the true position of the picture elements. A moving picture or smaller screen size will also change the appearance of thermal noise.

In fact, when the video becomes unuseable at the picture tube because of the noise interference, then the signal to noise ratio at the detector can be considered the system limit. As far as the sync circuits are concerned, the received bandwidth can be reduced without seriously modifying the sync waveform. This will improve the signal to noise ratio for the sync signal with a corresponding reduction in the dynamic phase error under limiting conditions.

If we treat the syncs as a trapezoidal waveform, the contribution of each harmonic to the effective timing information can be calculated. This is shown in Figure 9 and it can be seen that 90% of the timing information is

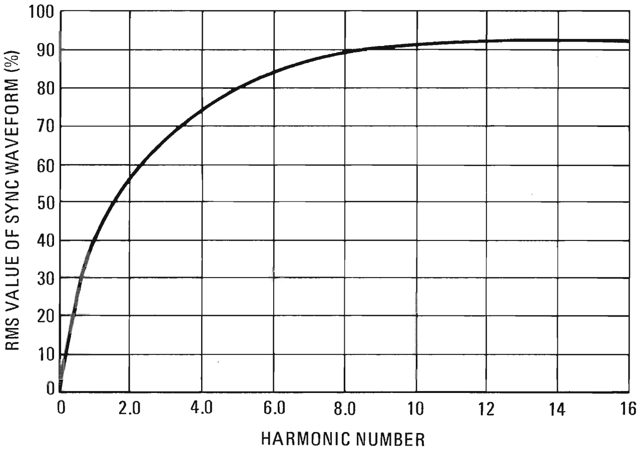

FIGURE 9

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(3)The reduction of the pull-in range vs. a.g.c. loop frequency response has been dealt with in the literature. However, the use of fast sync separators and the superior characteristics of I/C a.g.c. loops will probably make further investigation academic in nature.

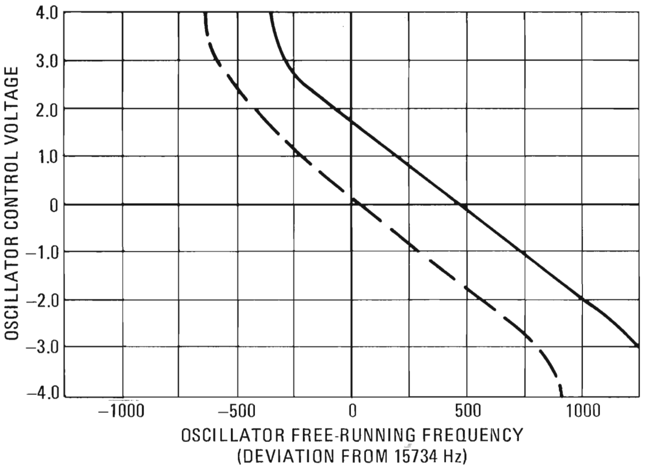

FIGURE 10 (a)

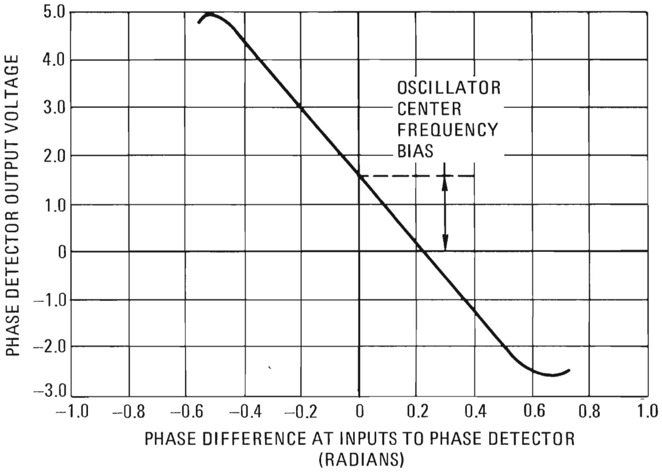

FIGURE 10 (b)

contained in the first nine harmonics of 15.734 KHz—a bandwidth of approximately 140 KHz. The bandwidth of many tube and hybrid designs has been as low as 100 KHz (determined primarily by the sync separator device) and this provides 87% of the available timing information with good thermal noise immunity. A typical solid state receiver has a bandwidth in excess of 1 MHz (determined by the circuits preceding the sync separator) and the noise bandwidth of the APC/AFC loop may have to be reduced, or further filtering in the sync channel *before* sync separation may be necessary to provide comparable thermal noise performance.

The approach to an APC/AFC design for a television receiver can take several different paths. For example: The design problem may simply be modification of a circuit to remove an undesirable characteristic caused by a faulty design, production spreads or a new operating environment. Cost reduction may be the objective, or adaptation of an existing circuit to a new chassis design.

Should any of the above conditions be encountered, the best starting point is to fully evaluate the fundamental characteristics of the present circuit. This naturally includes measurements of the oscillator and phase detector sensitivities. Those are usually quite simple to make and may require just disconnecting the phase detector output from the voltage (or current) controlled device in the oscillator circuit. Sometimes the loading of the oscillator circuit on the phase detector may have to be duplicated (particularly with solid state circuits) or the effect of loading allowed for. Since linear operation of practical circuits is rarely encountered, the characteristics should be measured over the expected operating range of each block.

Figure 10(a) and (b) shows the measured sensitivity curves of a solid state monochrome receiver. In this particular case, asymmetrical pull-in was the problem and the cause is the change in oscillator sensitivity producing a fall in d.c. loop gain as the oscillator free-running frequency is lowered. Relocation of the d.c. operating point of the oscillator at 15.734 KHz is the solution (the dotted line on Figure 10).

Notice that the product of the two slopes will give the circuit d.c. loop gain. This will define the Static Phase Error as the oscillator drifts. For this particular circuit, a drift of ± 180 Hz would produce an S.P.E. of ±1 μs. Clearly, if this design were to be adapted to a color receiver, the loop gain would have to be raised. Obviously, the amount of loop gain increase required will depend on the drift characteristics of the loop. Before any efforts are made to change the loop gain, the oscillator frequency variation with temperature and supply voltage should be measured and the effects of aging estimated. The lower operating ambient temperature of a solid state set means that the temperature/frequency drift can be held to less than ±190 Hz, including the turn-on warm-up drift. Wherever possible, if increased loop gain is still needed, the most stable circuit block should be changed or increased drift will result.

When further cost reduction will seriously impair the circuit performance, or the circuit already cannot meet the full performance capability of the simple APC/AFC loop, other circuits or a complete new design may have to be investigated.

One excellent solution to the problem of low cost combined with full performance can be provided by an integrated circuit, either in combination with other circuit functions or simply as an APC/AFC block. Several I/C's performing this function are available and one circuit, the MC1391P, will be used to demonstrate the use and universality of the preceding theoretical analysis. The MC1391P is well suited for this purpose as its parameters are stable and well documented. Although it is an I/C, it is very flexible with an external filter and externally adjustable loop gain allowing any performance characteristic, within the limits of the simple APC/AFC loop, to be obtained. (See Figure 11 and Appendix)

The operating characteristics of the MC1391 are easily calculated (Ref. 5), or they can be measured. The oscillator sensitivity is best expressed in amps per radian as this is a current controlled device, and can be measured by disconnecting the phase detector output (pin 5) and noting the current through the filter resistor R into the oscillator timing pin (pin 7). This current can be positive or negative corresponding to the direction of the oscillator frequency offset. Note, however, that the oscillator sensitivity is dependent on the impedance at pin 7 and can be increased by raising the value of the timing resistor (with a concomitant reduction in the capacitor value to keep the same time constant). This is the method by which the circuit loop gain can be changed to suit the design aims.

Since the oscillator characteristic around the centre frequency of 15.734 KHz is very linear, the phase detector sensitivity can be determined simply by producing a known phase error between the sync and flyback pulses and noting the resulting oscillator free-running frequency to produce this error when the phase detector is disconnected. The measured oscillator characteristic will then indicate the phase detector offset current for this phase error. In a more general case, the oscillator characteristic may not be linear (see Figure 10a) and the above method would not give a direct evaluation of the phase detector characteristic and a more complicated method must be resorted to. A typical set-up is shown in Figure 11 where a generator is used to provide the flyback pulse and is also phase-locked to a second generator which provides the sync pulse. By using the advance/delay pulse output from the second generator, the inputs to the phase detector can be varied by known phase differences and the detector output current measured. This method has the additional advantage that any loading by the oscillator on the phase detector is retained for a true operating characteristic. The phase detector characteristic of the MC1391 is also very linear with the end points occurring at the edges of the sync pulse as this is a sync gated detector. Notice that the operating range of the diode detector in Figure 10 is nearly ±6 μs—or the flyback pulse width. For that loop, the stable operating region is determined partially by the oscillator characteristic rather than wholly by the phase detector as it is with the MC1391.

Once the phase detector characteristic is known, it is an easy matter to select the oscillator impedance for the oscillator sensitivity required to produce sufficient circuit d.c. loop gain. How much loop gain is sufficient will depend on several factors.

Primarily, there must be enough gain to maintain the Static Phase Error within defined limits, ideally ±0.5 μs for a flyback pulse gated chroma channel. Because the oscillator section of the MC1391 is designed for a nominal zero temperature coefficient, the free-running frequency can drift in either direction from 15.734 KHz. Over a 30^{o}C operating temperature range, the drift can be as much as ±25 Hz. The external frequency determining elements will add another ±75 Hz drift if the hold control is typically 10% of the total timing resistance (polystyrene and polyster capacitor ±100 p.pm/^{o}C, Cermet Pot 150 ppm/^{o}C and NC5 resistor). Apart from temperature drift of the oscillator an S.P.E. can be caused by the permissible transmitter tolerance for f_H, and sometimes CCTV applications must be considered, adding another 20 to 30 Hz. Finally, operator error must be included, that is the possibility of an incorrectly set hold control either by the factory or by the serviceman/customer.

The advantage of an R-C oscillator, from the I/C designer's viewpoint, is that both timing and oscillator control can be achieved with a single pin-out. For the set

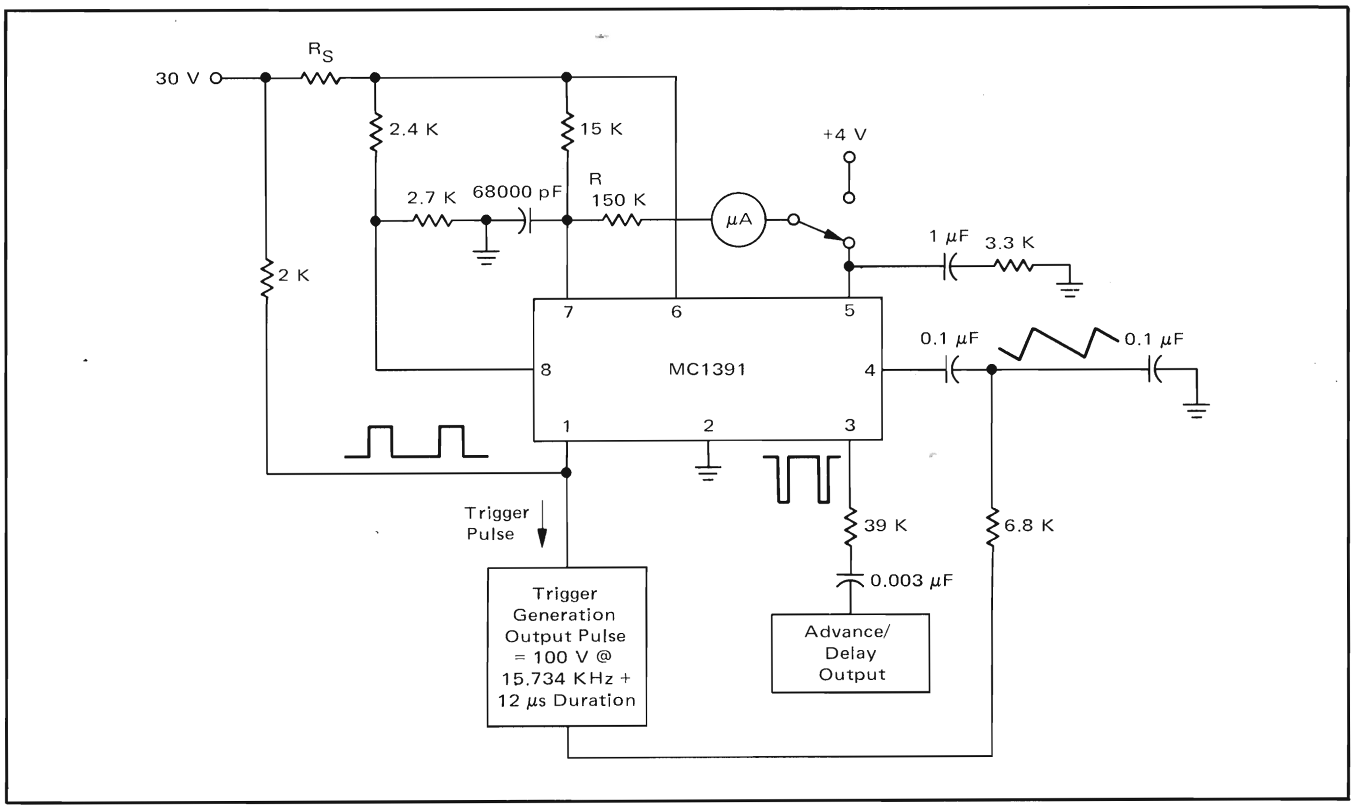

FIGURE 11 — Test Set-up for Measuring Oscillator and Phase Detector Characteristics

manufacturer, it avoids the use of a large inductor that may be subject to pick-up from toroidal yokes, for example. However, unless an expensive multiturn pot is used, the entire operating range of the oscillator is covered in a 320° rotation of the hold control. If the control capability is ±750 KHz, then each degree of rotation will change the oscillator frequency by 4.7 Hz. When an L-C oscillator is used, the t.p.i. of the inductor core can be used to limit the frequency change for a single 360° rotation of the hold control, thus making a relatively insensitive setting.

Worst Case Oscillator Deviation From f_H	= Internal Temp Drift	+ External Component Drift	+ Transmitted Tolerance	+ Operator Error	
	= 25 Hz	+ 75 Hz	+ 30 Hz	+ 60 Hz	= 190 Hz

Notice that the warm-up drift is not included in the above figure. This is the drift that occurs during the first few minutes after turn on as the I/C package temperature stabilizes to the 25°C ambient. It is not included since the hold control is usually adjusted after this period and unless it exceeds the pull-in range of an 'instant on' receiver, it cancels out and is not noticed.

The *minimum* loop gain is now defined by the permissible phase error over this frequency duration. Use equation ① :

$$\frac{0.5 \times 2\pi}{63.5} = \frac{190}{f_c}$$

$$\therefore f_c = 3840 \text{ Hz/rad.}$$

The drift characteristic has also defined the minimum pull-in range that can be tolerated and usually, if other dynamic performance characteristics are to be satisfactory, the value of loop gain given above is insufficient to guarantee pull-in over ±190 Hz. Also, the oscillator sensitivity and the phase detector sensitivity are subject to component tolerance and manufacturing tolerance and the loop gain must be in excess of 3800 Hz/rad to ensure that the S.P.E. will be maintained below 0.5 μs. It is a safe assumption that at least 50% more loop gain than the minimum will be needed.

$$\therefore f_c = \mu\beta = 6000 \text{ Hz/rad.}$$

Now the frequency deviation can be as much as ±300 Hz for acceptable phase performance.

The phase detector sensitivity of the MC1391 is nominally:

$$\mu = 1.6 \times 10^{-4} \text{ A/rad.}$$

(assuming a sync pulse deviation of 4.7 μs,
i.e., $\phi_s = 4.7 \times 0.095 = 0.46$ rads.)

Therefore, the required oscillator sensitivity $\beta = 37.3 \times 10^6$ Hz/A.

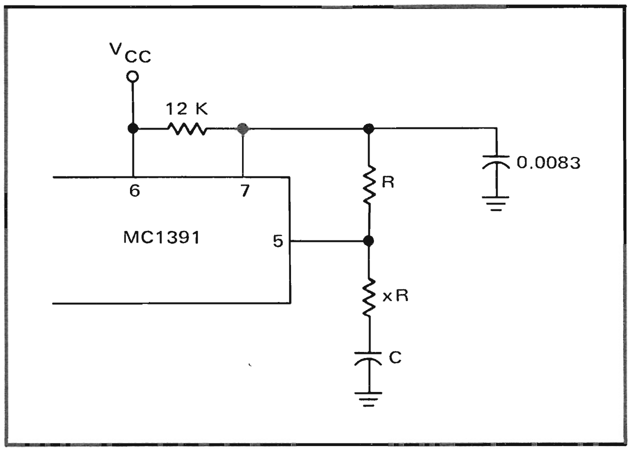

FIGURE 12 – MC1391 Filter Circuit

To obtain this sensitivity, the timing resistor at pin 7 must be 12 KΩ when the free-running frequency is 15.734 HKz, which will give a timing capacitor value of:

$$C = \frac{10^{-4}}{12 \times 10^{-6}} = 0.0083\ \mu\text{F}$$

The next part of the design procedure, the filter network, can appear somewhat arbitrary in nature as this is the area in which a designer can emphasize one performance characteristic but only at the expense of others.

Before making a first-cut try at the design, it should be noted that the resistor R between pins 5 and 7 can have a significant effect on the loop other than its function as part of the filter.

Earlier it was stated that the stable operating region of the phase detector in the MC1391 is confined to the width of the sync pulse. With the value of loop gain chosen previously, this means that the hold-in range of the oscillator can be as much as:

$$\frac{\pm 2.35 \times 2\pi \times 6000}{63.5} \simeq \pm 1400 \text{ Hz}$$

and obviously if higher loop gains are needed for the synchronous performance, it will become possible for the oscillator free-running frequency to deviate even more from 15.734 HKz at the hold-in limits. The full hold-in range can be realized, of course, only if the loop remains linear over the stable operating region. Should the value of R be large, then the available voltage swing at pin 5 will not permit the full phase detector current to be applied to pin 7, i.e., the phase detector will saturate. Reducing the hold-in frequency limit can be desirable and making the value of R fairly large to do this is a useful technique. (For a discrete circuit actively shaping the reference sawtooth to increase its slope or using limiting diode clamps on the oscillator control pin will have the same effect.)

When a step input phase change is applied to the loop, the response should be as rapid as possible to reach the new equilibrium. Two characteristics of the loop will define how far it can respond, the natural resonant frequency

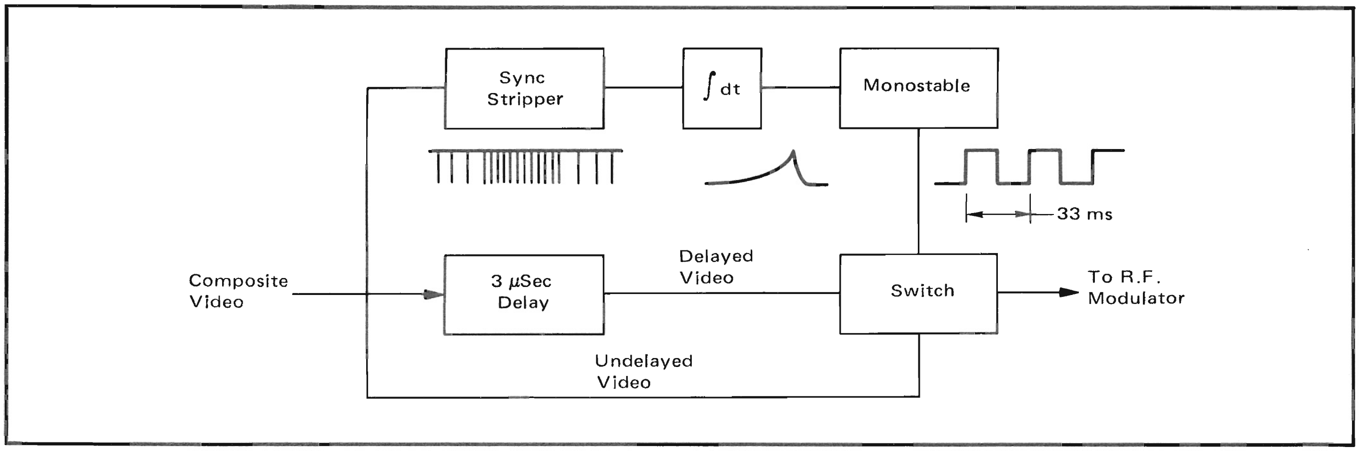

FIGURE 13 – Jitter Generator

and the amount of overshoot permitted when the correct phase has been reached. Both of these characteristics can be ideally demonstrated by using a Jitter Generator. This generator is inserted into the video channel of the r.f. modulator used to supply a signal to the receiver and it introduces (typically) a 3 μs delay during one field and then switches back to an undelayed signal on the next field.

This switching between delayed signal and undelayed signal will cause a vertical line in the video to trace the transient response of the loop on the CRT of the receiver. A typical response is shown in Figure 14.

An ideal response would be one that approached equilibrium as fast as possible without overshooting or 'hunting.' This indicates that the damping should be critical and the natural resonant frequency high, but this will result in a system with high a-c loop gain corresponding to large noise bandwidths. The effect of a fast recovery with lower natural resonant frequencies and acceptable noise bandwidths can be obtained by allowing some overshoot to occur. Usually the recovery from the transient should be complete within 1/3 to 1/2 of the field scan period. If a single overshoot is permitted, this will tend to limit the natural resonant frequency to a maximum of 363 Hz or 250 Hz, respectively (more than one overshoot during the recovery time indicates high natural resonant frequencies and large noise bandwidths with the chance of ringing to occur on impulse noise).

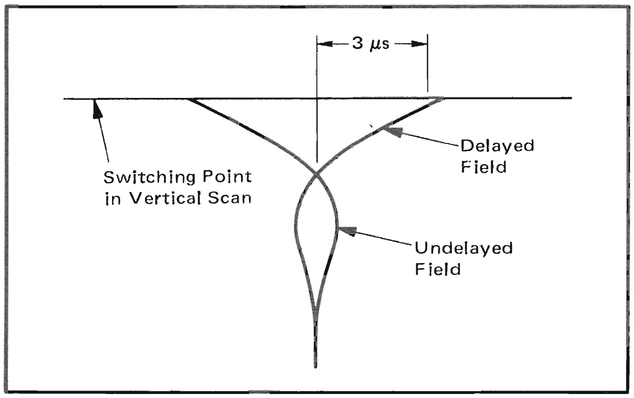

FIGURE 14 – Typical Transient Display on a CRT

Choosing a high natural resonant frequency of 250 Hz means that x should be selected to minimize the noise bandwidth.

From equation ⑤ :

$$\frac{d}{dx}(f_{nn}) = -\frac{1}{4\,x^2 T} + \frac{W_c}{4} = 0 \text{ for a minimum.}$$

i.e., $x = \sqrt{\frac{1}{W_c T}}$

From equation ⑧, this produces a value of 0.25 for K.

$W_c = 2\pi x 6000 = 37699$ rads/sec. volt

and $W_n = 2\pi x 250 = 1571$ rads/sec

If x is small, then $W_n \simeq \sqrt{\frac{W_c}{T}}$

$$\therefore T = \frac{37699}{(1571)^2} = \underline{0.0153}$$

$$\therefore x = \frac{1}{\sqrt{37699 \text{ x } 0.0153}} = \underline{0.0417}$$

$$\therefore m = \frac{x}{x+1} = \underline{0.04}$$

If we decide to limit the hold-in range to ±1 KHz then the linear operating region of the phase detector ϕ must be limited to:

$$\phi = \frac{2000}{f_c} = 0.33 \text{ radians}$$

The phase detector average current change = $\mu\phi_s$ =

$$1.61 \text{ x } 10^{-4} \text{ x } 0.33 = 0.053 \text{ mA}$$

Since the available voltage swing at pin 5 before saturation occurs is 5.8 V, then:

$$R = \frac{5.8}{0.053 \times 10^{-3}} \simeq 110\ K\Omega$$

$$\therefore \underline{\text{Put } R = 100\ K\Omega;}\ \therefore xR = 4.2\ K \underline{\simeq 3.9\ K\Omega}$$

With these practical values, x = 0.039 and m = 0.038

$$C = {}^{T}/_{R} = \underline{0.15\ \mu F}$$

The maximum possible pull-in range is given by equation ⑭ :

$$\Delta f = \pm \frac{2 \times 0.46 \times 6000 \sqrt{0.038}}{3 + 0.038}$$

$$\underline{= \pm\ 354\ Hz}$$

From equation ⑤ :

$$f_{nn} = \frac{1 + (0.039)^2 \times 0.015 \times 37699}{4 \times 0.039 \times 0.015}$$

$$= 795\ Hz$$

The response time to recover from a step input is given by:

$$t = \frac{\log_n 0.1}{-a} \qquad \text{where} \qquad a = \frac{1 + xT_{wc}}{2(1+x)T}$$

$$\text{i.e.,} \quad \underline{t = 3\mu s} \qquad\qquad = 739.6$$

This example effectively shows the compromises involved in the design of an APC loop. In aiming for a fast responsive loop with a quick recovery time to give optimum tracking of incoming phase variations (airplane flutter, etc.), we have obtained a loop with a noise bandwidth about twice what it should be. The stability of the sync when the incoming signal is heavily contaminated with thermal noise may be considered unsatisfactory; a continual jitter or "rubber banding" will be evident on the CRT. Also, because of the high a-c gain and very low damping of the loop, impulse noise will cause 'tearing' as the loop attempts to follow the transient changes produced by the impulse noise.

To improve the design with respect to the noise performance, several things can be done—the problem is to decide which changes will have the least effect on the other loop characteristics.

If the AC/DC gain ratio is reduced by changing x, the pull-in range will be reduced also. A safer course is to decrease the natural resonant frequency of the loop by modifying T, and a suitable design is shown in Figure 15.

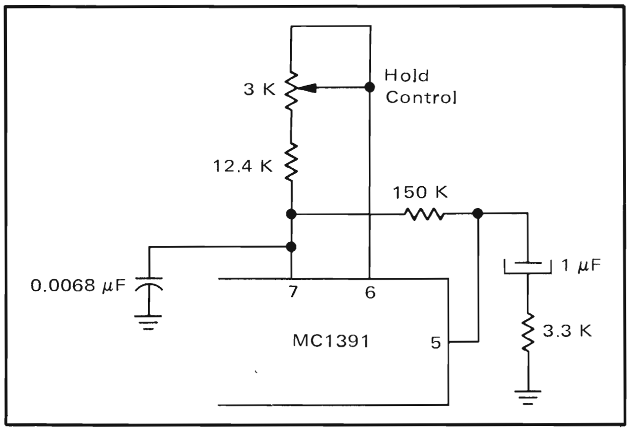

FIGURE 15

The d.c. loop gain has been increased slightly to:

$$f_c = \frac{1.61 \times 10^{-4} \times 13.9 \times 10^3 \times 15734}{5}$$

$$= 7040\ Hz/rad.$$

To limit the hold-in range to ±1 KHz,

$$\underline{R = 150\ K\Omega} \qquad \underline{xR = 3.3\ K\Omega}$$

$$x = 0.022 \qquad \therefore\ m = 0.0215$$

$$T = RC = 1X10^{-6} \times 150 \times 10^3 = \underline{0.15}$$

The lower loop time constant reduces the natural resonant frequency to 85 Hz and the damping coefficient K = 0.8.

$$f_{nn} = 1 + \frac{(0.022)^2\ 0.15 \times 2\pi \times 7040}{4 \times 0.022 \times 0.15} = \underline{319\ Hz}$$

The pull-in range is slightly lower at ±315 Hz, and the recovery time from a step transient is 4.8 μs.

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3. **HEROTA, NABEYAMA, MIYAZAKI**
"Design and Analysis of the Pull-In Range of Horizontal AFC in Television Systems"
4. **RICHMAN, D.**
"Color Carrier Reference Phase Synchronization Accuracy in the N.T.S.C. Color Television"
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5. **WILCOX, M.**
"A TV Horizontal I/C"

APPENDIX A

1 radian = 57.296 degrees

$f_H = 15.734$ KHz

$T = 63.5\ \mu$sec.

1 μs at $f_H = 5.699$ degrees = 0.0989 radians

APPENDIX B

Loop Recovery Time From a Step Transient.
The D.E. of the loop can be written:

$$p^2 + \frac{(1+xTw_c)p}{(1+x)T} + \frac{W_c}{(1+x)T} = 0$$

i.e., $p^2 + 2ap + c = 0$

The envelope
decay = $K_e{}^{-at}$

The envelope decay = $K_e{}^{-at}$

where K is proportional to the initial step amplitude.

$$\therefore a = \frac{1+xTw_c}{2(1+x)T}$$

Therefore, the time to decay to 10% of the initial offset is given by:

$$e^{-at} = 0.1$$

$$\therefore t = \frac{\log_n 0.1}{-a}$$

$$= \frac{2.303}{(1+xTw_c) \Big/ 2(1+x)T}$$

APPENDIX C

Spectrum of the Horizontal Sync Waveform.

For a trapezoidal waveform of amplitude A, period T and duration t_o with rise and fall times of t_1 then:

$$A_{rms} = A\sqrt{\frac{3t_o+2t_1}{3T}} \qquad A_{avg} = A\frac{(t_o+t_1)}{T}$$

$$= A \times 0.278$$

Amplitude of the nth harmonic:

$$A_n = 2A_{avg}\left\{\frac{\sin\pi n t_1/T}{\pi n t_1/T} \bullet \frac{\sin\pi n\left(\frac{t_1+t_o}{T}\right)}{\pi n\left(\frac{t_1+t_o}{T}\right)}\right\}$$

$$= A\ 0.1575 \times \frac{\sin(0.0124n)\sin(0.247n)}{3.06 \times 10^{-3} \times n^2}$$

Calculating the contribution of each harmonic to the total effective value generates the curve shown in Figure 9.

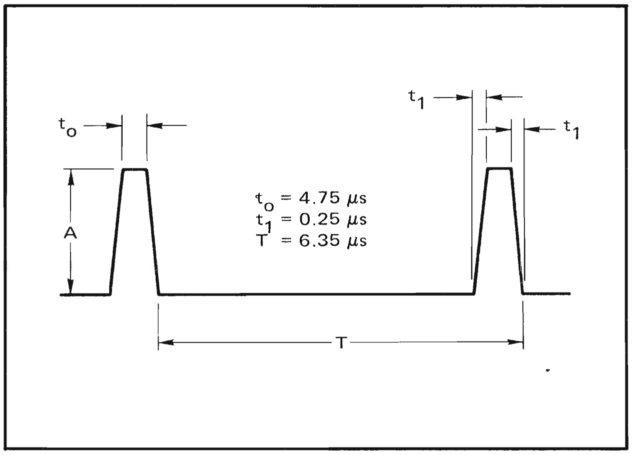

FIGURE C-1

APPENDIX D

Circuit Diagram of the MC1391.

The output pulse width is adjusted by the resistive divider at pin 8. For stable operation, the impedance at pin 8 should be close to 1 KΩ. To advance the static phasing, a small resistor (<100 Ω) can be placed between the flyback pulse integrating capacitor and ground.

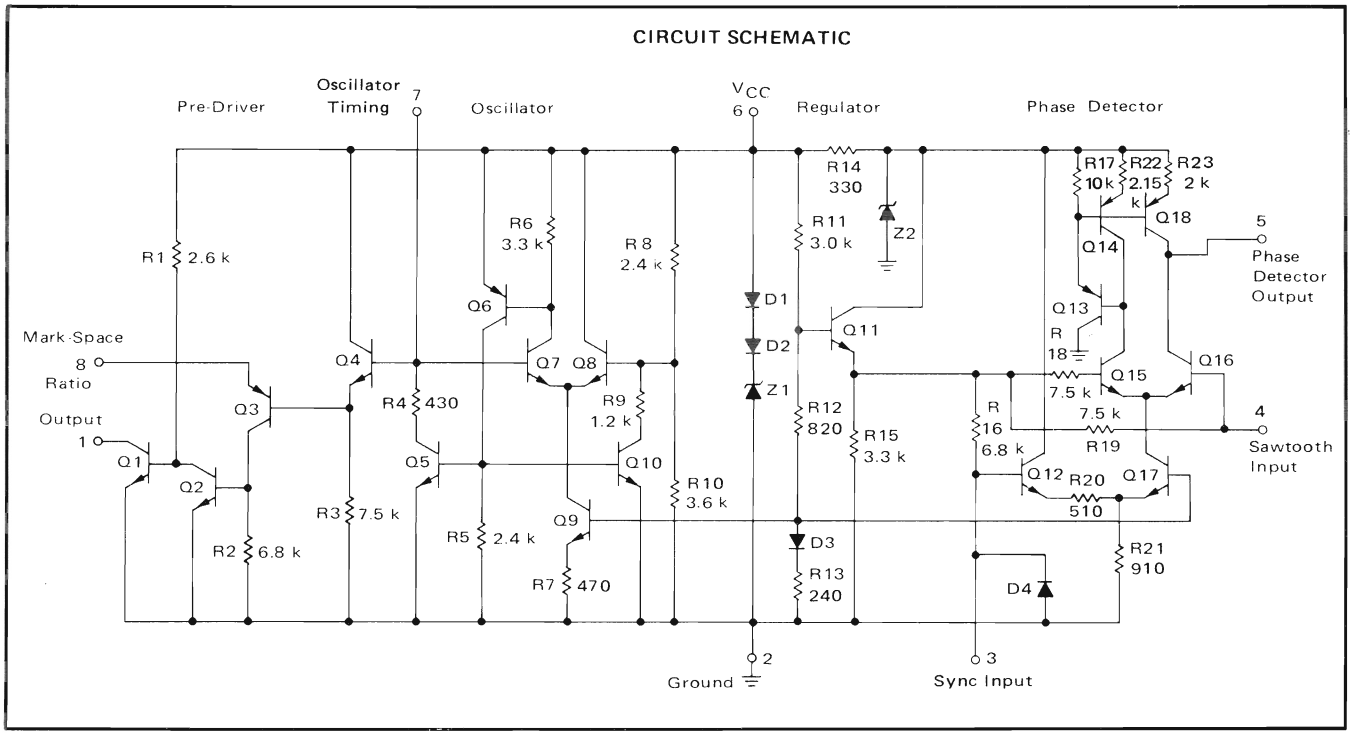

FIGURE D-1

APPENDIX E

The MC1391 Oscillator Circuit.

If it is assumed that Q_7 is initially off, then the capacitor connected from pin 7 to ground will be charged by an external resistor (R_T) connected to pin 6. As soon as pin 7 voltage exceeds 5 V, the potential at Q_8 base, Q_7 will conduct allowing Q_6 to supply base current to Q_5 and Q_{10}. Transistor Q_{10} sets the base of Q_8 at approximately 2 V. Q_5 then discharges C_T through R_4 until pin 7 reaches 2 V and Q_7 turns off again and the cycle repeats.

The frequency of oscillation is given by:

$$f_o = \frac{1}{t_c l_n \left(1 + \frac{R_2{}^2}{R_1R_2 + R_1R_3 + R_2R_3}\right) + t_d l_n \left(1 + \frac{R_1R_2}{R_1R_3 + R_2R_3}\right)}$$

and for $f_o = 15.734$ KHz

$t_c \underline{\Omega} 10^{-4}$ if $R >> R4$

t_c = charge time constant = R_TC_T

t_d = discharge time constant = R_4C_T

For small frequency deviations, the oscillator sensitivity:

$$\beta = \frac{15.734 \times R_T}{5\ V} \quad Hz/A$$

The sensitivity can be adjusted by changing the external resistor R_T.

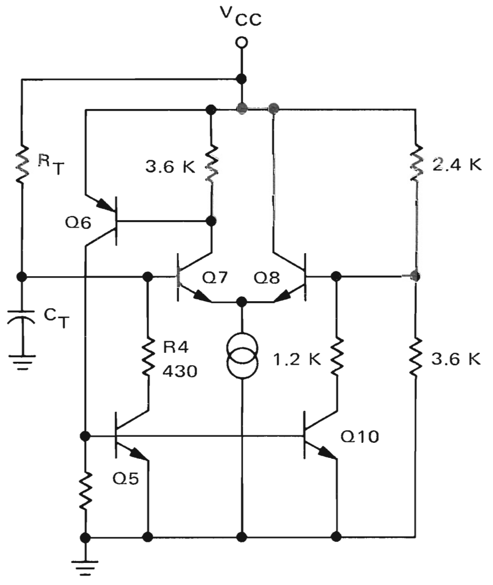

FIGURE E-1

APPENDIX F

Phase Detector Operation of the MC1391P.

The phase detector consists of the comparator Q_{15} and Q_{16} and the gated current source Q_{17}. Negative going sync pulses (1 V to 5 V $_{(p\text{-}p)}$) at pin 3 turn off Q_{12} allowing Q_{17} to conduct. The current division between Q_{15} and Q_{16} during the sync pulse period will be determined by the phase relationship between the syncs and the sawtooth at pin 4 which is derived from the horizontal flyback pulse. If the steep slope of the sawtooth is symmetrical about the sync pulse (Figure F2), then Q_{15} and Q_{16} will each conduct for half the sync pulse period. When the sawtooth is just less than 2 V, Q_{15} conducts all the Q_{17} current, and this current is turned around by Q_{18} to flow out of pin 5. When the sawtooth is above 2 V, Q_{16} conducts and current flows into pin 5; thus the net current at balance is zero. When a phase offset occurs, there will be an average current flow either in or out of pin 5 to speed up or slow down the oscillator. Note that if the sawtooth amplitude is greater than about 1 V $_{(p\text{-}p)}$, the change in voltage at pin 4 to completely switch the comparator is small compared to the amplitude of the saw. Switching can be considered instantaneous and the detector sensitivity is independent of either the sawtooth amplitude or the sync pulse amplitude.

The average phase detector current goes from zero to full output in half the sync pulse width:

$$\therefore \mu = \frac{(I_{peak} \text{ x duty cycle})}{(\text{conduction period})}$$

$$= \frac{0.5\text{x}10^{-3} \text{ x } \frac{4.7}{63.5}}{0.5 \text{ x } 4.7 \text{ x } 0.098} \text{ A/rad.}$$

If the sawtooth is reasonably linear, then the phase detector output current

$$\pm I = \mp \mu\phi$$

where ϕ is the phase difference between the oscillator and the sync pulse.

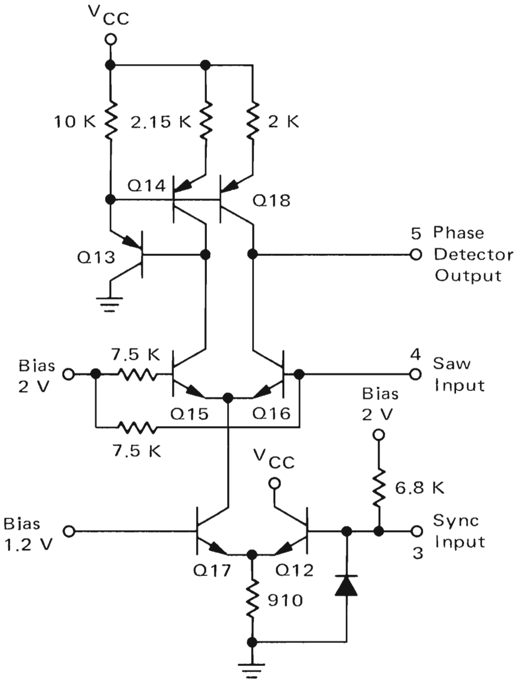

FIGURE F-1

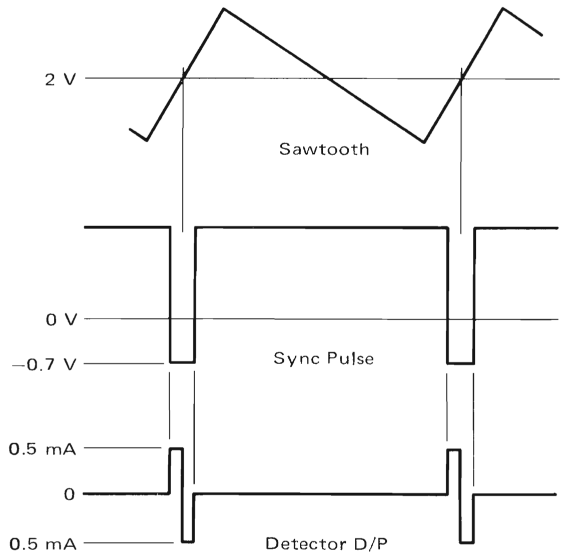

FIGURE F-2

APPENDIX G

Dual Diode Bridge Phase Detectors.

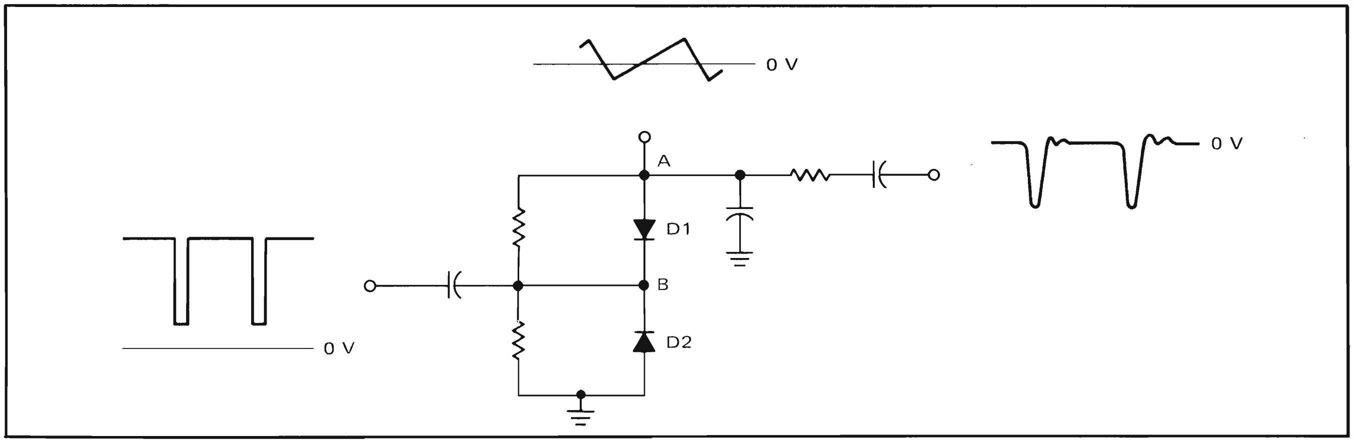

FIGURE G-1 – Diode Bridge

In the simple dual diode bridge phase detector, the negative going sync pulse tips are clamped to ground by D_2 and the waveform at B is shown in Figure G2(a). The output voltage from the bridge due to the sync waveform is very small because the diode D_1 is back biassed between the sync pulses (when B is very positive) and the impedance at A, determined largely by the integrating capacitor for the flyback pulse, is small compared to the diode load resistors. Therefore, when an a.c. coupled sawtooth is applied to A and the phase is such that the steep slope of the waveform is symmetrical about the sync pulse, the waveform at A is as shown in Figure G2(b). The bridge output is nominally zero. If the oscillator beings to lead the sync pulses, the sawtooth is clamped later on its steep portion as shown in G2(c) and a net +ve voltage is obtained. This voltage is filtered and applied to the control device to slow the oscillator down. Similarly for a lagging oscillator, a net –ve voltage is developed to speed the oscillator up (Figure G2(d)). Notice that the output voltage obtained is a maximum at each end of the sawtooth steep slope, i.e., the stable operating range is over the flyback pulse width. If the flyback pulse width is ϕ_s radians and the peak-to-peak sawtooth amplitude is E volts, then:

$$\mu = \frac{E}{\phi_s} \text{ volts/radian}$$

and the phase detector output voltage for a phase shift between oscillator and sync pulse of $\pm\phi$ is:

$$\pm E_{out} = \pm\mu\phi$$

Obviously, the phase detector sensitivity can be increased by increasing the reference sawtooth amplitudes (but not to the point where the sawtooth can start the diode D_1 into conduction–the saw amplitude must be less than the sync pulse amplitude). Alternatively increasing the slope (reducing ϕ_s) has the same effect. The simple diode detector is very dependent on the sawtooth shape and amplitude. If the sync amplitude is large, then the bridge is relatively independent of amplitude modulation of the syncs, but if these are heavily differentiated amplitude modulation will also cause phase modulation when the bridge is unbalanced.

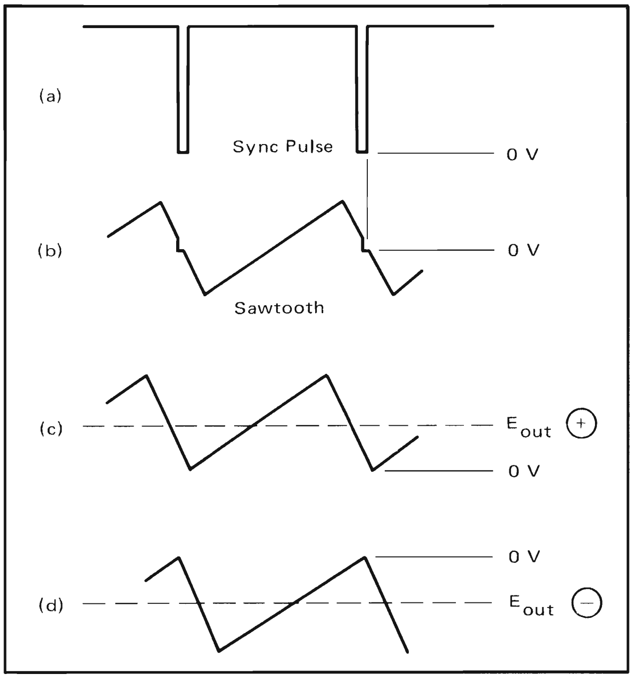

FIGURE G-2

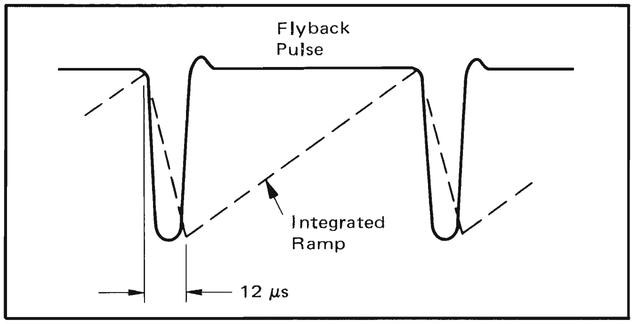

FIGURE G-3

APPENDIX H

Derivation of the Approximate Expression Given in Equation ⑩ for the Maximum Pull-In Range.

The general D.E. for the loop is:

$$p\phi + F_{(p)}\omega_c\phi = p\phi_i$$

which can be rewritten:

$$\frac{d\phi}{dt} + F_{(p)}\omega_c\phi = \Delta\omega \qquad \text{———— ⑪}$$

Now $F_{(p)} = \frac{1+pxT}{1+p(1+x)T} = \frac{1-m+pT}{1+m+pT}$

since $x = \frac{m}{m-1}$

$\therefore F_{(p)} = m + \left\{\frac{1-2m+m^2}{1-m+pT}\right\}$

Substituting this in equation ⑪ gives:

$$\frac{d\phi}{dt} + mw_c\phi + \left\{\frac{1-2m+m^2}{1-m+pT}\right\} \omega_c\phi = \Delta\omega$$

If we write $W_I = \Delta\omega - \left\{\frac{1-2m+m^2}{1-m+pT}\right\} \omega_c\phi$

then W_I is the effective instantaneous impressed frequency difference, produced by the detuning error of the oscillator ($\Delta\omega$) and the frequency drift generated by the correction voltage across the filter capacitor. As pull-in progresses the right-hand term will cause ω_I to be reduced, and the mean value of W_I

$$\overline{W_I} = \Delta\omega - \left\{\frac{1-2m+m^2}{1-m+pT}\right\} \omega_c\phi$$

Since the capacitor bias is generated by applying the mean phase detector output $m\omega_c\overline{\phi}$ to the filter

$$\overline{W_I} \approx \Delta\omega - \left\{\frac{1-2m+m^2}{1-m+pT}\right\} \omega_c\overline{\phi}$$

Now $\frac{d\phi}{dt} + m\omega_c\phi = W_I$ ———— ⑫

If it is assumed that the average bias across the filter capacitor will not change significantly during a cycle of the beat-note (i.e., the filter time constant is long compared to the beat-note frequency), we can find this average bias by integrating the loop D.E. over a cycle of the beat-note.

Integrating ⑫ over the beat note period T_{BN}:

$$\int_t^{t+T_{BN}} \frac{d\phi}{dt}\,dt + \int_t^{t+T_{BN}} m\omega_c\phi = \int_t^{t+T_{BN}} W_I$$

$$-2\pi + \int_t^{t+T_{BN}} m\omega_c\phi = -\overline{W_I}T_{BN}$$

The integral in the above equation is the area under a cycle of phase detector output and this integral, divided by the beat note period will give the mean d.c. component of the output:

i.e., $-\overline{m\omega_c\phi} = -\overline{W_I} + \overline{W_{BN}}$

$\therefore$ The mean d.c. component $\overline{\omega_c\phi} = \frac{1}{m}\left\{\overline{W_I} - \overline{W_{BN}}\right\}$ ⑬

When the phase detector generates a cycle of the beat note in the time T_{BN}, it will have operated in two regions—the stable region for a time t_s and the unstable region for a time t_u such that:

$$\frac{1}{T_{BN}} = \frac{1}{t_s + t_u}$$

Solving equation ⑬ in the region ϕ_s:

$$\int_0^{t_s} m\omega_c dt = \int_{-\phi_s/2}^{+\phi_s/2} \frac{d\phi}{\frac{W_I}{m\omega_c} - \phi}$$

$$\therefore m\omega_c t_s = \left[\log_e\left(\frac{W_I}{m\omega_c} - \phi\right)\right]_{-\phi_s/2}^{+\phi_s/2}$$

$$\therefore t_s = \frac{1}{m\omega_c}\log_e\left\{1 + \frac{2}{\frac{2W_I}{m\omega_c\phi_s} - 1}\right\}$$

Similarly during ϕ_u:

$$\frac{m\omega_c\phi_s t_u}{\phi u} = \log_e\left\{1 + \frac{2}{\frac{2W_I}{m\omega_c\phi_s} - 1}\right\}$$

$$\therefore W_{BN} = \frac{2\pi}{T_{BN}} = \frac{m\omega_c\phi_s}{\log_e\left\{1 + \frac{2}{\frac{2W_I}{m\omega_c\phi_s} - 1}\right\}} \qquad \phi_s + \phi_u = 2\pi$$

Substituting this expression into E_y ⑫ gives

$$\omega_c\overline{\phi} = \frac{1}{m}\left\{\overline{W_I} - \frac{m\omega_c\phi_s}{\log_e\left[1+\left(\dfrac{2}{\dfrac{2W_I}{m\omega_c\phi_s}-1}\right)\right]}\right\} \quad ⑭$$

Now:

$$\overline{W_I} = \Delta\omega - \left\{\frac{1-2m+m^2}{1-m+pT}\right\}\overline{\omega_c\phi}$$

$$\therefore \omega_c\phi = \left[\frac{1-m+pT}{1-2m+m^2}\right]\Delta\omega-\overline{W_I}$$

$$= \frac{\Delta\omega}{(1-m)} - \frac{\overline{W_I}}{(1-m)} - \frac{T}{(1-m)^2}\frac{d}{dt}\overline{W_I}$$

using partial fractions and noting T = RC = const.

Substituting equation ⑭ in the above:

$$\overline{W_I} - \frac{m\omega_c\phi_s}{\log_e\left\{1+\left(\dfrac{2}{\dfrac{2W_I}{m\omega_c\phi_s}-1}\right)\right\}} = \frac{m\Delta\omega}{(1-m)}$$

$$-\frac{m\overline{W_I}}{(1-m)} - \frac{m}{(1-m)^2}T\frac{d}{dt}\overline{W_I}$$

Putting $K = \frac{2\overline{W_I}}{\omega_c\phi_s}$ representing the average frequency difference

and $K_0 = \frac{2\Delta\omega}{\omega_c\phi_s}$ representing the initial frequency difference

and multiplying the equation by $\frac{(1-m)^2}{m\,\omega_c\,\phi_s}$

$$(1-m)K - \frac{2(1-m)}{\log_e\left(\frac{K+1}{K-1}\right)} = K_o - mK - \frac{m}{1-m}T\frac{dk}{dt}$$

or

$$\left(\frac{1-m}{mT}\right)dt = \frac{dK}{K_o - K + \dfrac{2(1-m)}{\log_e\left(\frac{K+1}{K-1}\right)}}$$

If the mean average frequency (K) decreases with time then the initial frequency difference (K_o) is within the pull-in range. Putting T_F for the limit time to pull-in from $\overline{W_I} = \Delta\omega$ to $\overline{W_I} = \frac{m\omega_c\phi_s}{2}$

$$\left(\frac{1-m}{mT}\right)T_F = \int_{\frac{K_o}{m}}^{1}\frac{dK}{K_o - K + \dfrac{2(1-m)}{\log_e\left(\frac{K+1}{K-1}\right)}}$$

In the limit, if T_F is real:

$$K_o - K + \frac{2(1-m)}{\log_e\left(\frac{K+1}{K-1}\right)} > 0$$

or

$$K_o = \left\{K - \frac{2(1-m)}{\log_e\dfrac{K+1}{K-1}}\right\} \quad \text{limit}$$

For a maximum,

$$\frac{d}{dk}(K_o) = 0 = 4(1-m)-(K-1)(K+1)\left\{\log_e\left(\frac{K+1}{K-1}\right)\right\}^2$$

$$\log_e(K+1)-\log_e(K-1) = 2\left\{\frac{1}{K}+\frac{1}{3K^3}+\frac{1}{5K^5}+\dots\right\}$$

$$\therefore 4(1-m) \approx (K+1)(K-1)\,4\left(\frac{1}{K^2}\right) \quad \text{if } (K) > 1$$

i.e., $K = \frac{1}{\sqrt{m}}$

$\therefore K_o$ (max)

$$= \frac{1}{\sqrt{m}} - \frac{2(1-m)}{\log\left(\frac{1}{\sqrt{m}}+1\right) - \log\left(\frac{1}{\sqrt{m}}-1\right)}$$

$$= \frac{1}{\sqrt{m}} - \frac{2(1-m)3}{2\sqrt{m}(3+m)} \quad \text{if } m \ll 1$$

$$= \frac{4\sqrt{m}}{(3+m)}$$

$$\therefore \Delta\omega_{max} = \frac{\phi_s\omega_c}{2}\,\frac{4\sqrt{m}}{(3+m)}$$

i.e., Maximum pull-in range $\Delta f_{max} = \frac{2\phi_s f_c\sqrt{m}}{(3+m)}$ ⑪

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